IN THE CLAIMS:

1 (original). A semiconductor device comprising:

at least one memory cell configured to generate a first voltage on a first bit line and including a switching device having a first resistance;

at least one reference cell configured to generate a second voltage on a second bit line and including:

a first resistive element coupled between a voltage source and the second bit line and having a second resistance; and

a second resistive element coupled between a sink and the second bit line and having a third resistance; and

a sense amplifier for generating an output in response to the first and the second voltages.

2 (new). The semiconductor of claim 1 wherein at least one of the first and the second resistive elements comprises a transistor.

3 (new). The semiconductor of claim 1 wherein each of the first and the second resistive elements comprises a transistor.

4 (new). The semiconductor of claim 1 wherein the memory cell comprises a NDR and an access device.

5 (new). The semiconductor of claim 4 wherein the NDR comprises a thyristor.